LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A semiconductor wafer comprising:

a semiconducting or non-semiconducting substrate;

a buried insulator layer located on an upper surface of the substrate;

an intermediate adhesion layer located on an upper surface the buried insulator layer; and

a Ge-containing layer having an exposed upper surface located on an upper surface of the intermediate adhesion layer, wherein said intermediate adhesion layer provides a bond between said buried insulator layer and said Ge-containing layer and eliminates Ge-oxide from said wafer and said Ge-containing layer represents the uppermost layer of the wafer.

Claim 2 (Withdrawn) The semiconductor wafer of Claim 1 wherein a surface of the Ge-containing layer that is in contact with the intermediate adhesion layer is roughened.

Claim 3 (Original) The semiconductor wafer of Claim 1 wherein said substrate is a semiconducting substrate which comprises a semiconductor selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP and other III/V or II/VI compound semiconductors.

Claim 4 (Original) The semiconductor wafer of Claim 1 wherein said substrate is a Si-containing semiconductor substrate selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, Si/SiGeC and preformed silicon-on-insulators.

Claim 5 (Original) The semiconductor wafer of Claim 1 wherein said substrate comprises strained layers, unstrained layers or a combination thereof.

Claim 6 (Original) The semiconductor wafer of Claim 1 wherein said buried insulator layer is a crystalline or non-crystalline oxide, nitride or combination thereof.

Claim 7 (Original) The semiconductor wafer of Claim 1 wherein said buried insulator layer comprises SiO_2.

Claim 8 (Withdrawn) The semiconductor wafer of Claim 1 further comprising a buried diffusive mirror located in between the buried insulator layer and another buried insulator.

Claim 9 (Withdrawn) The semiconductor wafer of Claim 8 wherein the buried diffusive mirror is corrugated.

Claim 10 (Withdrawn) The semiconductor wafer of Claim 9 wherein the buried diffusive mirror comprises a metal.

Claim 11 (Original) The semiconductor wafer of Claim 1 wherein said intermediate adhesion layer is a Si material.

Claim 12 (Original) The semiconductor wafer of Claim 11 wherein said Si material is single crystal Si, polycrystalline Si, amorphous Si, epitaxial Si or combinations and multilayers thereof.

Claim 13 (Original) The semiconductor wafer of Claim 1 wherein said Ge-containing layer is a pure Ge layer.

Claim 14 (Original) The semiconductor wafer of Claim 1 wherein said Ge-containing layer is a thin layer having a thickness from about 1 nm to about 1000 nm.

Claim 15 (Withdrawn) A semiconductor wafer comprising:

a substrate;

a Bragg mirror located on said substrate; and

a Ge-on-insulator film located on said Bragg mirror, wherein said Bragg mirror comprises a plurality of two alternating dielectric films.

Claim 16 (Withdrawn) The semiconductor wafer of Claim 15 wherein said Bragg mirror comprises a plurality of alternating layers of SiO_2 and Si_3N_4.

Claim 17 (Withdrawn) A semiconductor wafer comprising

a semiconducting or non-semiconducting substrate;

a buried insulator layer located on an upper surface of the substrate; and

a Ge-containing layer located on an upper surface of the buried insulator layer, wherein said Ge-containing layer is attached to the buried insulator film by a roughened surface.

Claim 18 (Withdrawn) The semiconductor wafer of Claim 17 wherein said substrate is a semiconducting substrate which comprises a semiconductor selected from the group consisting

of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP and other III/V or II/VI compound semiconductors.

Claim 19 (Withdrawn) The semiconductor wafer of Claim 17 wherein said substrate is a Si-containing semiconductor substrate selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, Si/SiGeC and preformed silicon-on-insulators.

Claim 20 (Withdrawn) The semiconductor wafer of Claim 17 wherein said substrate comprises strained layers, unstrained layers or a combination thereof.

Claim 21 (Withdrawn) The semiconductor wafer of Claim 17 wherein said buried insulator layer is a crystalline or non-crystalline oxide, nitride or combination thereof.

Claim 22 (Withdrawn) The semiconductor wafer of Claim 17 wherein said buried insulator layer comprises SiO_2.

Claim 23 (Withdrawn) The semiconductor wafer of Claim 17 wherein said buried insulator layer is a Bragg mirror having at least a pair of alternating dielectric layers of different refractive indices.

Claim 24 (Withdrawn) The semiconductor wafer of Claim 17 further comprising a buried diffusive mirror located in between the buried insulator layer and another buried insulator.

Claim 25 (Withdrawn) The semiconductor wafer of Claim 24 wherein the buried diffusive mirror is corrugated.

Claim 26 (Withdrawn) The semiconductor wafer of Claim 25 wherein the buried diffusive mirror comprises a metal.

Claim 27 (Withdrawn) The semiconductor wafer of Claim 17 wherein said Ge-containing layer is a pure Ge layer.

Claim 28 (Withdrawn) The semiconductor wafer of Claim 17 wherein said Ge-containing layer is a thin layer having a thickness from about 1 nm to about 1000 nm.

Claim 29 (Original) A semiconductor structure comprising at least the semiconductor wafer of Claim 1 and at least one device or circuit located thereon.

Claim 30 (Original) The semiconductor structure of Claim 29 wherein the device is a Ge-photodetector.

Claim 31 (Original) The semiconductor structure of Claim 29 wherein the circuit is a Si-containing circuit.

Claim 32 (Original) The semiconductor structure of Claim 29 wherein said device or said circuit is monolithically integrated.

Claim 33 (Withdrawn) A semiconductor structure comprising at least the semiconductor wafer of Claim 17 and at least one device or circuit located thereon.

Claim 34 (Withdrawn) The semiconductor structure of Claim 33 wherein the device is a Ge-photodetector.

Claim 35 (Withdrawn) The semiconductor structure of Claim 33 wherein the circuit is a Si-containing circuit.

Claim 36 (Withdrawn) The semiconductor structure of Claim 33 wherein said device or said circuit is monolithically integrated.

Claims 37-68 (Cancelled)